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PATENT NUMBER and  
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## U.S. UTILITY Patent Application

38919.0-8 PTO  
12/061517  
81731/03

APPL NUM 10061517	FILING DATE 01/31/2002	CLASS <del>324</del> 714	SUBCLASS 704	GAU <del>2853</del>	EXAMINER <i>[Signature]</i>
<b>**APPLICANTS:</b> Harres Daniel; 2133 <div style="text-align: right;"><u>KCR VEROS</u></div>					
<b>**CONTINUING DATA VERIFIED:</b> <i>look at 6/9/2004</i>					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> <i>None 8/9/2004</i>					
PG-PUB <input type="checkbox"/>		DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		ATTORNEY DOCKET NO 091-0124	
Verified and Acknowledged Examiners's initials		<i>[Signature]</i>			
TITLE : Built-in test signal attenuation circuit					

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for O.G.
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg. Print Fig.
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>Application Examiner</b>	
		<b>PREPARED FOR ISSUE</b>	
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